CLAIMS:

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1. Integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween; the high K capacitor dielectric region comprising a high K substantially amorphous material layer and a high K substantially crystalline material layer.

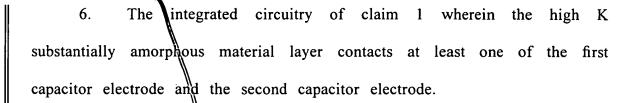
- 2. The integrated circuitry of claim 1 wherein the high K substantially amorphous material and the high K substantially crystalline material constitute the same chemical composition.
- 3. The integrated circuitry of claim 1 wherein the high K substantially amorphous material and the high K substantially crystalline material constitute different chemical compositions.
- 4. The integrated circuitry of claim 1 wherein at least one of the first and second electrodes comprises elemental metal, metal alloy, conductive metal oxides, or mixtures thereof.
- 5. The integrated circuitry of claim 1 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

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- 7. The integrated circuitry of claim 6 wherein the high K substantially amorphous material layer contacts only one of the first capacitor electrode and the second capacitor electrode.
- 8. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer contacts one of the first and second capacitor electrodes and the high K substantially crystalline material layer contacts the other of the first and second capacitor electrodes.
- 9. The integrated circuitry of claim 1 wherein the high K capacitor dielectric region is the only capacitor dielectric region received between the first and second capacitor electrodes, and consists essentially of the high K substantially amorphous material layer and the high K substantially crystalline material layer.
- 10. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer is at least 98% amorphous, and the high K substantially crystalline material layer is at least 98% crystalline.

- 11. The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially crystalline material layer being received between the semiconductor substrate and the high K substantially amorphous material layer.
- 12. The integrated circuitry of claim 11 wherein the semiconductor substrate comprises bulk monocrystalline silicon.
- 13. The integrated circuitry of claim 11 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.
- 14. The integrated circuitry of claim 11 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.
- 15. The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially amorphous material layer being received between the semiconductor substrate and the high K substantially crystalline material layer.



16. The integrated circuitry of claim 15 wherein the semiconductor substrate comprising bulk monogrystalline silicon.

Integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a ${\rm Ta_2O_5}$ comprising capacitor dielectric region received therebetween; the ${\rm Ta_2O_5}$ comprising region comprising a substantially amorphous ${\rm Ta_2O_5}$ comprising layer and a substantially crystalline ${\rm Ta_2O_5}$ comprising layer.

- 18. The integrated circuitry of claim 17 wherein at least one of the substantially amorphous Ta₂O₅ comprising layer contacts at least one of the first capacitor electrode and the second capacitor electrode.
- 19. The integrated circuitry of claim 17 wherein the substantially amorphous Ta₂O₅ comprising layer contacts at least one of the first capacitor electrode and the second capacitor electrode.
- 20. The integrated circuitry of claim 19 wherein the substantially amorphous Ta₂O₅ comprising layer contacts only one of the first capacitor electrode and the second capacitor electrode.

- 21. The integrated circuitry of claim 17 wherein the substantially amorphous Ta₂O₅ comprising layer contacts one of the first and second capacitor electrodes and the substantially crystalline Ta₂O₅ comprising layer contacts the other of the first and second capacitor electrodes.
- 22. The integrated circuitry of claim 17 wherein the Ta_2O_5 comprising region is the only capacitor dielectric region received between the first and second capacitor electrodes, and consists essentially of the substantially amorphous Ta_2O_5 comprising layer and the substantially crystalline Ta_2O_5 comprising layer.
 - 23. A capacitor: forming method comprising:

forming a first capacitor electrode layer over a substrate;

forming a high K capacitor dielectric region over the first capacitor electrode layer, the high K capacitor dielectric region comprising a high K substantially crystalline material layer and a high K substantially amorphous material layer; and

forming a second capacitor electrode layer over the high K capacitor dielectric region.

24. The method of claim 23 comprising forming the high K substantially amorphous material and the high K substantially crystalline material to constitute the same chemical composition.

25.	The	method	of	claim	24	wherein	the	chemical	composition
comprises	Ta ₂ O ₅ .								

- 26. The method of claim 23 comprising forming the high K substantially amorphous material and the high K substantially crystalline material to constitute different chemical compositions.
- 27. The method of claim 23 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode layer and the second capacitor electrode layer.
- 28. The method of claim 23 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode layer and the second capacitor electrode layer.
- 29. The method of claim 28 wherein the high K substantially amorphous material layer contacts only one of the first capacitor electrode layer and the second capacitor electrode layer.
- 30. The method of claim 23 wherein the high K substantially amorphous material layer contacts one of the first and second capacitor electrode layers and the high K substantially crystalline material layer contacts the other of the first and second capacitor electrode layers.

The method of claim 23 wherein the high K capacitor dielectric region is formed to be the only capacitor dielectric region received between the first and second capacitor electrode layers, and consists essentially of the high K substantially amorphous material layer and the high K substantially crystalline material layer.

32. The method of claim 23 wherein the high K substantially amorphous material layer is formed to be at least 98% amorphous, and the high K substantially crystalline material layer is formed to be at least 98% crystalline.

33. A capacitor forming method comprising:

forming a first capacitor electrode layer over a substrate;

depositing a substantially amorphous first high K capacitor dielectric material layer over the first capacitor electrode layer;

converting the substantially amorphous high K first capacitor dielectric material layer to be substantially crystalline;

after the converting, depositing a substantially amorphous second high K capacitor dielectric material layer over the substantially crystalline first high K capacitor dielectric material layer; and

forming a second capacitor electrode layer over the substantially amorphous second high K capacitor dielectric material layer.

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- 34. The method of claim 33 further comprising after the converting and before forming the second capacitor electrode layer, oxidize annealing the second high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C and effective to maintain the second high K capacitor dielectric material layer substantially amorphous.
- 35. The method of claim 33 further comprising after the converting and before forming the second capacitor electrode layer, oxidize annealing the second high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of from about 300°C to about 550°C and effective to maintain the second high K capacitor dielectric material layer substantially amorphous.
- 36. The method of claim 33 wherein the converting occurs in an atmosphere which is substantially void oxygen.
- 37. The method of claim 33 wherein the first and second dielectric material layers are formed to constitute the same chemical composition.
- 38. The method of claim 37 wherein the chemical composition comprises Ta₂O₅.

- 39. The method of claim 33 wherein the first and second dielectric material layers are formed to constitute different chemical compositions.
- 40. The method of claim 33 wherein the second capacitor electrode layer is formed to contact the substantially amorphous second high K capacitor dielectric material layer.
- 41. The method of claim 33 wherein the first high K capacitor dielectric material layer is formed to contact the first capacitor electrode layer.
- 42. The method of claim 33 wherein the first high K capacitor dielectric material layer is formed to contact the first capacitor electrode layer, and the second capacitor electrode layer is formed to contact the substantially amorphous second high K capacitor dielectric material layer.
- 43. The method of claim 33 wherein the first high K capacitor dielectric material layer is formed to contact the first capacitor electrode layer, the second high K capacitor dielectric material layer is formed to contact the first high K capacitor dielectric material layer, and the second capacitor electrode layer is formed to contact the second high K capacitor dielectric material layer.

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23 24 44. NA capacitor forming method comprising:

forming a first capacitor electrode layer over a substrate;

depositing a substantially amorphous first high K capacitor dielectric material layer over the first capacitor electrode layer;

oxidize annealing the first high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C;

after the oxidize annealing of the first high K capacitor dielectric material layer, converting the substantially amorphous high K first capacitor dielectric material layer to be substantially crystalline;

after the converting, depositing a substantially amorphous second high K capacitor dielectric material layer over the substantially crystalline first high K capacitor dielectric material layer;

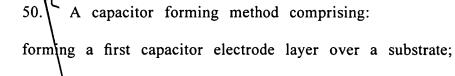
oxidize annealing the second high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C and effective to maintain the second high K capacitor dielectric material layer substantially amorphous; and

forming a second capacitor electrode layer over the substantially amorphous second high K capacitor dielectric material layer.

45. The method of claim 44 further wherein the first and second oxidize annealings comprise annealing in an oxygen containing atmosphere at a temperature of no greater than about 600°C.

46.	The	method	of cl	laim 44	wherein	the	converting	occurs	in	ar
atmosphere	which	is subs	tantial	ly void	oxygen.					

- 47. The method of claim 44 wherein the first and second dielectric material layers are formed to constitute the same chemical composition.
- 48. The method of claim 47 wherein the chemical composition comprises Ta₂O₅.
- 49. The method of claim 44 wherein the first and second dielectric material layers are formed to constitute different chemical compositions.



depositing a substantially amorphous first high K capacitor dielectric material layer over the first capacitor electrode layer;

converting the substantially amorphous high K first capacitor dielectric material layer to be substantially crystalline;

after the converting of the substantially amorphous high K first capacitor dielectric material layer, oxidize annealing the first high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C;

after the oxidize annealing of the first high K capacitor dielectric material layer, depositing a substantially amorphous second high K capacitor dielectric material layer over the substantially crystalline first high K capacitor dielectric material layer,

oxidize annealing the second high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C and effective to maintain the second high K capacitor dielectric material layer substantially amorphous; and

forming a second capacitor electrode layer over the substantially amorphous second high K capacitor dielectric material layer.

51. The method of claim 50 further wherein the first and second oxidize annealings comprise annealing in an oxygen containing atmosphere at a temperature of no greater than about 600°C.

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52. The method of claim 50 wherein the converting occurs in an atmosphere which is substantially void oxygen.

- 53. The method of claim 50 wherein the first and second dielectric material layers are formed to constitute the same chemical composition.
- 54. The method of claim 53 wherein the chemical composition comprises Ta_2O_5 .
- 55. The method of claim 50 wherein the first and second dielectric material layers are formed to constitute different chemical compositions.

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